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Function requirement of electronic design automation software

电子设计自动化软件功能要求

(English Translation)

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Contents

Foreword

This document is drafted in accordance with the rules set forth in GB/T 1.1-2020 *Directives for standardization -- Part 1: Rules for the structure and drafting of standardizing documents.*

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This is the first release.

Function requirement of electronic design automation software

1 Scope

This document specifies the operation environment of electronic design automation software and the basic requirement of product design functions.
This document can be used in research ,development and testing of the electronic design automation software product for analogic and RF design.

2 Normative References

There are no normative references in this document.

3 Terms,Definitions and Abbreviations

The following terms、definitions and abbreviations apply to this document.

3.1 Terms and Definitions

3.1.1
electronic design automation
EDA,the design method which uses computer-aided design software to complete the simulation design flow of functional design,physical design (including arrangement,wiring,layout,design rule checking,etc.) and validation.

3.1.2
electronic design automation software
the software tools which are mainly used to complete a series of processes such as circuit simulation design,functional simulation,layout design, extraction of parasitic parameter of circuit and physical verification ,and finally output design data.

3.1.3
layout
a geometric description of real circuit physical conditions.

3.1.4
application program interface(API)
the standard program interface uses to exchange information and commands for EDA tools.

3.2 Abbreviation

DRC (Design Rule Check)
ERC (Electrical Rules Check)
GDS (Graphical Data System file)
LVL (Layout vs. Layout)
LVS (Layout vs. Schematic)

PDK (Process Design Kit)
PVE (Physical Verification Explorer)
RCE (RC Extraction)

4 Runtime environment requirements

4.1 Local system

EDA tools are installed on the local server with the Linux system environment. The hardware configuration of the server shall have enough running memory, hard disk storage and processor ability to ensure the normal operation of EDA tools.

4.2 Cloud system

Cloud system refers to that the necessary functional modules are placed in the cloud server, such as:
a) Software authorization management module
Supporting the License sales model, lease model, and charging by volume model for adaptive cloud sales.
b) The standard device library
For components and PDK processes used in design, establish cloud-based device library, PDK library management and version management.
Note: In principle, offline version libraries are no longer available for customers to use, which ensure standardization of device and processes in design processes, and effectively support design manufacturability on specified version libraries.

5 Functional requirements

5.1 General flow framework

EDA Operation Flow Framework are shown in figure 1, include:
File management module: be responsible for the import and export of data documents, the establishment and storage of library files and the management of process documents
View functional module: can adjust the operation interface and zoom the viewing area.
Creation and Edit module: can create and edit various graphics (circuit design、layout design).
Verification functional module: provide the layout verification tools to check the design rules and the uniformity between layout and schematic.
Layer operation module: can enter different layers of cells for operation.
Hierarchy operation module: can enter different hierarchies for operation
Query module: can provide distance, angle, area measurement and trace net
Automatic routing module: can automatically route and connect the devices in the layout according to the nodes.
RC extraction module: can extract the parasitic resistance and capacitance parameters.
Simulation module: can conduct circuit simulation.
API interface function module: The API supports extended programming.

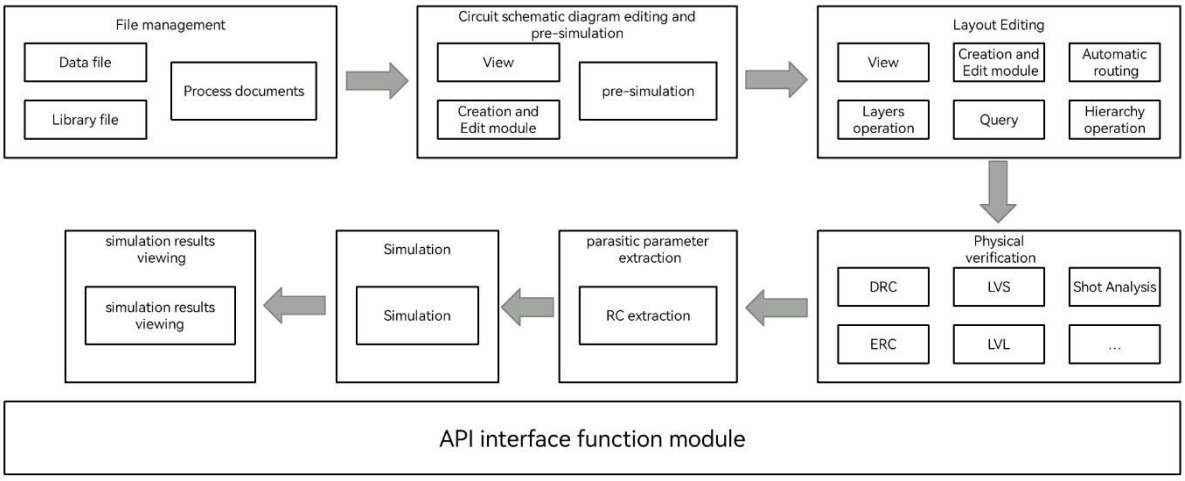

Figure 1　EDA Operation Flow Framework

The specific process is as follows:

a) Import and create a new data and process file through the file management module;

b) When editing the schematic diagram, adjust the operation interface and zoom the view area through the view module, and generate the schematic diagram through the creation and edit module

c) After editing the schematic diagram, the pre-simulation operation can be carried out to verify the correctness of the circuit schematic diagram;

d) When editing the layout, you can adjust the operation interface and zoom the view area through the view module, generate and modify the layout graphics through the creation and edit module, and modify the layout content through the layers operation module, hierarchy operation module, query module and automatic routing module;

e) After completing the layout design, the physical verification can be carried out to verify and check the content of the circuit schematic diagram and layout. If there is an error, the error will be located, and the step d) will be repeated to modify the error until the verification is passed

f) After the physical verification, the resistance and capacitance parameters of the layout are extracted;

g) Conduct circuit simulation based on parasitic parameter extraction results and schematic diagram. If the simulation results are wrong, return to step d) to modify the layout; If the simulation passes, the required data files can be output according to user requirements;

h) View the simulation result;

i) The API interface function module supports extended programming for API interface programming.

5.2　File management

This function supports the import, saving and export of the data file, the establishment of library files and management of process files. The detailed descriptions are shown in table 1.

table 1 The descriptions of the file management

Function		Description
Data file	Import	Import GDS/TF/DEF/LEF/EDIF/Design/Verilog/DXF/DSPF/SPICE/OASIS and other data
	Save	Save data file
	Export	Export GDS/TF/DEF/LEF/EDIF/Design/Verilog/DXF/DSPF/SPICE/OASIS and other data
	New	New Library/Cell file
Process documents	Import	Import、save and export technology file
	Save	
	Export	

5.3 View

This function supports the switching, zooming in and out of the interface windows. The detailed descriptions are shown in table 2.

table 2 The descriptions of the view

Function	Description
Windows operating	Support window opening and closing
Window adjustment	Supports display, zoom, etc. of the content user selected
Locate	Support the location of the points or graphics
Display Depth	Support for display level control
Multi window management	Support simultaneous operation of multiple windows

5.4 Creation and Edit

This function support the creation and editing of various graphics in circuit and layout design, the detailed descriptions are shown in table 3.

table 3　The descriptions of the creation and edit

Function		Description
Create	Circuit diagram generation (Schematic design)	Introduce electronic components and generate interconnections between them to generate the Circuit schematic diagram.
	Graphic generation (Layout design)	Create the graphics such as Rectangle/Polygon/Circle/Ellips/Arc/Donut/ Instance/Label/Pin/Wire/DimensionRuler and other object unit
Edit	Undo/Redo	Undo and redo the last operation
	Copy、Paste、Move、Delete	Copy, paste, move and delete the selected drawing objects
	Circuit schematic diagram editing (Schematic design)	Stretch, rotate, mirror, align, and array the selected drawing objects
	Layout Editing (Layout design)	
	Special processing (Layout design)	Support smooth corner、metal slot、metal fill and other operations
	Find/Replace/ Select (Layout design)	Support customize search criteria, objects and ranges for search and replacement; Support the selection of objects such as layer by frame selection.
	Property modification	Supports view and modification of selected object properties, connection settings and parameters
	Advanced operations (Layout design)	Supports graphics merging, Boolean operations, graphics generation from operations, graphics expansion/reduction, etc
	Other editing functions (toolbox)	Adjust spacing/Path width/quickly generate graphics/bus connections, etc.

5.5　Verification

This function can realize comprehensive verification and check of layout quickly and locate errors accurately to ensure the correctness of layout. The detailed descriptions are shown in table 4.

table 4　The descriptions of the verification

Function	Description
DRC	Check whether the layout conforms to the process rules, for example, check whether the line spacing, line width, etc. meet the process requirements
LVS consistency check	Check the consistency between circuit schematic diagram and layout
ERC	Check for electrical rule violations such as short circuit and open circuit
LVL	Check the consistency between the layout and the layout, and effectively locate the layout difference units and graphics
PVE	Support DRC, LVS, ERC and LVL operation results summary, classification and viewing; Support accurate back-annotating of operation results to schematic diagram or layout

5.6 Layers operation

Support users to operate on the selected layer, the detailed descriptions are shown in Table 5.

table 5　The descriptions of the layers operation

Function	Description
Hide Layers	Hide Selected Layers
Show Layer	Show Selected Layers
Layer Management	Support the addition and deletion of layers
Layer Editing	Support the settings such as the color and filling of the layers

5.7 Hierarchy operation

This function supports user to enter different hierarchies for editing. The hierarchy refers to a unit in the design. The detailed descriptions are shown in table 6.

table 6　The descriptions of the hierarchy operation

Function	Description
Hierarchical skip	Enter the lower cell / return to the upper cell
Make Cell and Smash	Support the merging of scattered graphics or devices into the same cell; Support to break up cell contents
Clone Master	Copy and update a referenced cell
Show Tree	Show the tree reference structure in the current cell

5.8 Query

This function can query layout design information, such as measuring layout size, trace net, etc. The detailed descriptions are shown in table 7.

table 7 The descriptions of the query

Function	Description
Ruler	Support building and clearing of ruler
Measure	Support the measurement of distance, width, length, angle, perimeter, area, Path length.
Probe Layer	Support prompt, selection and switching for overlapping layers
Trace Net	Support routing tracing of nodes in the layout

5.9 Automatic routing

This function supports automatic routing according to user’s routing strategy. The example of wiring command is shown in Table 8.

table 8 The descriptions of the automatic routing

Function	Description
Point to point routing	Support to specify two ports for point-to-point routing
Multipoint routing	Support one-to-many or many-to-many port automatic routing

5.10 RC extraction

This function provides resistance and capacitance extraction function.
The detailed descriptions are shown in table 9.

table 9 The descriptions of the RC extraction

Function	Description
RC extraction and caculation	Supports the extraction and calculation of resistance and capacitance of the layout
resistance and capacitance viewer	View the resistance and capacitance extraction results

5.11 Simulation and simulation results viewing

The simulation module provides circuit simulation tools and simulation result viewing tools, the main contents are shown in table 10.

table 10　The descriptions of the simulation

Function	Description
Simulation	Use simulation tools to call/simulate circuit schematic diagram or netlist, include time-domain, frequency-domain simulation
Result viewing and data processing	Use the viewing tool to display the simulation results as oscillograms and handle the data

5.12　API interface function

The API supports extended programming.

5.13　Other necessary information

This part provides the user manual and version information of the software. The main contents are shown in table 11.

table 11　Other necessary information

Necessary information	Description
Manual	Provide the user manual of the EDA software, including function introduction, method of application, etc
Version Overview and Release Notes	Provide the EDA software version information and update content
Access page	Provide official websites